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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/820,580	04/08/2004	Stephen L. Morein	00100.02.0003	8567

29153 7590 04/26/2007

ADVANCED MICRO DEVICES, INC.
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EXAMINER	
NGUYEN, HAU H	
ART UNIT	PAPER NUMBER
2628	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/820,580	MOREIN ET AL.	
	Examiner	Art Unit	
	Hau H. Nguyen	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) *1-11* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on February 23, 2007 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 12-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Fu et al. (U.S. Patent No. 6,825,848, hereinafter, Fu).

As per claim 12, Fu teach a memory architecture as shown in Fig. 1, comprising:

a level one cache (15), comprising texel information;

a level two cache (13), coupled to the level one cache (15) that comprises overlapping fetched texel information resulting from execution of previous memory fetch instructions (*i.e., L2 cache contains texel information that is not in the L1 cache, in other words, L1 cache returns with a miss, and L2 cache return with a hit of the requested texel*, Figs. 14 and 15);

wherein when the level one cache does not comprise overlapping fetched texel information requested by a subsequent memory fetch information (*subsequent memory fetch result with a miss in L1 cache*), the level two cache is operative to transmit the overlapping fetched texel information requested by the subsequent memory fetch instruction to the level one cache (steps 175-179, Fig. 15); and

wherein each of the previous memory fetch instructions and the subsequent memory fetch instruction result in storage of requested texel information at least in the level one cache (Fig. 15, step 179, col. 14, line 55 to col. 15, line 7).

As per claim 13, Fu teach the level one cache comprises a plurality of texture cache blocks (Fig. 7), wherein one of the plurality of texture cache blocks is operative to receive the subsequent texel fetch instruction (such as, from L2 cache as cited above).

As per claim 14, Fu further teach the memory architecture comprising a main memory (3, Fig. 1) operative coupled to the level two cache (13), and wherein when the level one cache and the level two cache do not comprise texel information requested by a second subsequent memory fetch instruction, the main memory is operative to transmit the texel information requested by the second subsequent memory fetch instruction to the level two cache (col. 15, lines 8-20).

As per claim 15, Fu also teach after the texels are transferred from the main memory to the level two cache, the transferred texels in the level two cache is then transferred to the level one cache (col. 15, lines 14-20).

As per claim 16, Fu teach a graphics processing device (Fig. 1) comprising:

a graphics controller (such as, graphics engine 17) operative to execute memory fetch instruction (execute texels fetched in L1 cache, col. 15, lines 20-25);

a main memory (3, Fig. 1);

a level one cache coupled to the graphics controller, the level one cache comprising texel information (Fig. 1, and as cited above with reference to claim 12);

a level two cache coupled between the main memory and the level one cache, the level two cache comprising overlapping fetched texel information resulting from execution of previous memory fetch instruction (Fig. 1, and as cited above with reference to claim 12);

wherein when the level one cache does not comprise overlapping fetched texel information requested by a subsequent memory fetched instruction, the level two cache transmits the overlapping fetched texel information requested by the subsequent memory fetch instruction to the level one cache; and

wherein each of the previous memory fetch instructions and the subsequent memory fetch instruction result in storage of requested texel information at least in the level one cache (as cited above with reference to claim 12).

As per claim 17, Fu further teach the graphics controller is operative to request the subsequent memory fetch instruction (*the graphics engine 17 request memory fetch instruction to the L1 cache for data to be processed*, col. 13, lines 34-38, and col. 15, lines 20-25).

As per claim 18, Fu teach the graphics controller comprising a plurality of fetch blocks, wherein one of the plurality of fetch blocks is operative to request the subsequent memory fetch instruction (*such as obtaining adjacent texels*, col. 15, line 66 through col. 16, line 10).

As per claim 19, as cited above, the level one cache transmits the overlapping fetched texel information requested by the subsequent memory fetch instruction to the graphics

controller (e.g. in case when the L1 cache contains all the requested texels (step 173, Fig. 15), all the requested texels are transferred to the graphics engine 17 for processing as cited above).

Claim 20, which is similar in scope to claim 13, is thus rejected under the same rationale.

Claim 21, which is similar in scope to claim 14, is thus rejected under the same rationale.

Claim 22, which is similar in scope to claim 15, is thus rejected under the same rationale.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hau H. Nguyen whose telephone number is: 571-272-7787. The examiner can normally be reached on MON-FRI from 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on (571) 272-7794.

The fax number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

H. Nguyen

4/24/2007

KEE M. TUNG
SUPERVISORY PATENT EXAMINER